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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,922	12/02/2003	Deva N. Pattanayak	VISH-8728	8797

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 01/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/726,922	PATTANAYAK ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *02 December 2003*.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-26* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/02/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:

   I. Claims 1-10 and 24-26, drawn to a semiconductor device, classified in class 257, subclass 327.

   II. Claims 11-23, drawn to a method of making semiconductor devices, classified in class 438, subclass 212.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions II and I are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the product as claimed could be made by a materially different process, for example by forming the semiconductor layer around trench regions by selective deposition, or by doping the first semiconductor layer before depositing the second semiconductor layer into the plurality of trenches.

3. Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

4. During a telephone interview with Eric Gash on 01/07/05 a provisional election was made without traverse to prosecute the invention of Group I, claims 1-10 and 24-26. Affirmation of this election must be made by applicant in replying to this Office action. Claims 11-23 are

withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Claim Rejections - 35 USC § 112

6. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

7. Claims 2 and 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Specifically, the specification does not refer to "a low gate-to-drain capacitance on resistance product."

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-6, 8-10 and 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Saito et al. (US 2004/0195618 A1).

In re claim 1, Saito (esp. Fig. 1) discloses a semiconductor device, comprising:

a drain region (11);

a body region (12a) disposed above said drain region;

a gate region (24a-2) disposed within said body region;

a gate insulator region (23a; Fig. 12) disposed about a periphery of said gate region;

a plurality of source regions (13a) disposed along the surface of said body region proximate a periphery of said gate insulator region;

wherein a first portion of said gate region (24a-1) and a first portion of said gate insulator region are formed as a substantially parallel elongated structure;

wherein a second portion of said gate region (24a-2) and a second portion of said gate insulator region are formed as a normal-to-parallel structure;

wherein a first portion of said drain region overlaps said parallel structure; and

wherein a second portion of said drain region is separated from (by semiconductor region 14B) said normal-to-parallel structure.

In re claim 2, as best understood, Saito discloses the device of claim 1, wherein said device provides a low (decreased) gate-to-drain capacitance (section [0072], lines 13-17). The "on resistance," as best understood is comparable to that of the instant application based on the similarity of structure between the Saito structure and that of Applicant's Prior Art (Fig. 2), described on pp. 6, lines 8-12) of Applicant's specification.

In re claim 3, Saito discloses the device of claim 1, wherein said closed cell MOSFET provides a reduced gate-to-drain capacitance gate-to-source capacitance ratio. This claim is met by the prior art Saito for the same reasons as the instant application, in that a low gate-to-drain capacitance will product a high gate-to-source capacitance (Applicant's specification pp. 15, lines 5-6). This, in turn, produces the claimed reduced ratio (pp. 15, lines 11-13). There is no reason why this same result will not be present with the structure of the prior art Saito.

In re claim 4, Saito discloses the device of claim 1, wherein said overlap of said first portion of said drain region and said parallel elongated structure comprises an extension of said drain region.

In re claim 5, Saito discloses the device of claim 1, wherein said separation of said second portion of said drain region and said normal-to-parallel elongated structure comprises a well (14B) of said body portion.

In re claim 6, Saito discloses the device of claim 1, wherein said body region (12a) and said plurality of source regions (13a) are electrically coupled together.

In re claim 8, Saito discloses the device of claim 1, wherein said drain region comprises:

a first drain portion (15) having a high doping concentration (section [0083], line 5); and

A second drain portion (11), having a low doping concentration (section [0083]), line 8), disposed between said body region (12) and said first drain region.

In re claim 9, Saito discloses the device of claim 8. The limitation, "wherein said second drain portion increases ... TMOSFET" is a recitation of the intended use of the claimed device. Terms that simply set forth the intended use, a property inherent in or a function, do not differentiate the claimed composition of these elements from those known to prior art.

In re claim 10, Saito discloses the device of claim 8, wherein

said first portion of said drain region comprises a heavily n-doped semiconductor; and

said second portion of said drain region comprises a lightly n-doped semiconductor.

In re claim 24, Saito (esp. Fig. 1) discloses a semiconductor device, comprising:

a plurality of open gate-drain regions (with gate 24a-2) arranged in a first plurality of parallel regions; and

a plurality of closed gate-drain regions (with gate 24-1) arranged in a second plurality of parallel regions normal to said open gate-drain regions.

In re claim 25, as best understood, Saito discloses the device of claim 24, wherein said device provides a low (decreased) gate-to-drain capacitance (section [0072], lines 13-17). The "on resistance," as best understood is comparable to that of the instant application based on the similarity of structure between the Saito structure and that of Applicant's Prior Art (Fig. 2), described on pp. 6, lines 8-12) of Applicant's specification.

In re claim 26, Saito discloses the device of claim 24, wherein said closed cell MOSFET provides a reduced gate-to-drain capacitance gate-to-source capacitance ratio. This claim is met by the prior art Saito for the same reasons as the instant application, in that a low gate-to-drain

capacitance will product a high gate-to-source capacitance (Applicant's specification pp. 15, lines 5-6). This, in turn, produces the claimed reduced ratio (pp. 15, lines 11-13). There is no reason why this same result will not be present with the structure of the prior art Saito.

Claim Rejections - 35 USC § 103

10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

11. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Saito as applied to claim 1 above, and further in view of Darwish et al. (US 2003/0062570 A1).

In re claim 7, Saito discloses the device of claim 1, whrein;

said drain region (11, 15) comprises an n-doped semiconductor (section [0082], lines 3-4);

said body region (12) comprises a p-doped semiconductor (section [0080]);

said gate insulator region (23a) comprises an oxide (section [0081]);

said plurality of source regions (13a) comprises a heavily n-doped semiconductor (section [0079], line 13), but does not expressly disclose said gate region comprising a heavily doped n-doped semiconductor. Darwish (esp. Fig. 3) discloses a heavily doped semiconductor polysilicon region (14) filling the gate trench (section [0024]). Darwish does not expressly disclose said gate layer comprising an N-type semiconductor. However, it would have been obvious for one skilled in the art at the time of the invention to select an N-type impurity rather

than a P-type impurity for the gate electrode for the purpose, for example, of enhancing the conductivity of the vertical channel region. This would be the obvious choice because both the source and drain regions are also N-type.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 571-272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jesse A. Fenty
Examiner
Art Unit 2815